WHAT IS CLAIMED IS:

- 1. A semiconductor device comprising:
- a lower buried oxide film disposed on a semiconductor substrate;
- a stress-relief film disposed on the lower buried oxide film;

an upper buried oxide film disposed on the stress-relief film; and

an SOI film disposed on the upper buried oxide film, wherein the SOI film is formed with a MOSFET having a source, a drain, and a channel, and

- a thermal expansion coefficient of the stress-relief film is greater than a thermal expansion coefficient of the upper buried oxide film.
- 2. The semiconductor device according to claim 1, wherein the stress-relief film is formed of a silicon film.
- 3. The semiconductor device according to claim 2, wherein the silicon film is formed of a crystal film, polycrystal film, or amorphous film, and the silicon film is a non-doped silicon film.
- 4. The semiconductor device according to claim 1, wherein the upper buried oxide film has almost a same film thickness as that of the SOI film, and the lower buried oxide film is thicker than the upper buried oxide film.
- The semiconductor device according to claim 1, wherein

the stress-relief film is formed of a composite film laminating a first silicon film, a germanium film disposed on the first silicon film, and a second silicon film disposed on the germanium film.

- 6. The semiconductor device according to claim 5, wherein the first and second silicon films of the composite film are formed of a crystal film, polycrystal film, or amorphous film, and the silicon film is a non-doped silicon film.
- 7. The semiconductor device according to claim 5, wherein the first and second silicon films of the composite film are thinner than the germanium film of the composite film.
- 8. The semiconductor device according to claim 1, wherein the thermal expansion coefficient of the stress-relief film is nearly equal to or greater than a thermal expansion coefficient of the SOI film.
- 9. A semiconductor device comprising: an insulating layer;
- a semiconductor layer disposed on the insulating layer; and
- a semiconductor element formed in the semiconductor layer,

wherein a stress-relief layer having a thermal expansion coefficient greater than a thermal expansion coefficient of the insulating layer is disposed at a position apart from a top of the insulating film contacting with the semiconductor

layer, and

the semiconductor layer and the stress-relief layer are disposed as a part of the insulating layer is interposed therebetween.

- 10. The semiconductor device according to claim 9, wherein a film thickness of the insulating layer interposed between the semiconductor layer and the stress-relief layer is almost the same as a film thickness of the semiconductor layer.
- 11. The semiconductor device according to claim 9, wherein the thermal expansion coefficient of the stress-relief layer is nearly equal to or greater than a thermal expansion coefficient of the semiconductor layer.
- 12. The semiconductor device according to claim 11, wherein the semiconductor layer and the stress-relief layer are formed of a same material.
- 13. The semiconductor device according to claim 12, wherein the semiconductor layer and the stress-relief layer are formed of a silicon film.
- 14. The semiconductor device according to claim 13, wherein the silicon film is any one of a non-doped single crystal silicon film, non-doped polysilicon film, or non-doped amorphous silicon film.
- 15. The semiconductor device according to claim 9, wherein the stress-relief layer includes a germanium film.
- 16. The semiconductor device according to claim 15, wherein

the stress-relief layer is configured of a composite film formed of the germanium film, a first silicon film disposed on the germanium film and contacting with the semiconductor layer, and a second silicon film disposed below the germanium film.